WHAT IS CLAIMED IS:

1. A memory device, comprising:

a data receive gate to buffer, in a first buffer, data to be inputted, by gate control;

a data transfer gate to input the data of said first buffer and buffer the same data in a second buffer by gate control;

a data write gate to output the data of said second buffer to a data bus by gate control;

a memory cell to write and store the data in said data bus;

a selector not to connect said data bus to said memory cell when masked by a data mask signal, and to connect the data bus to the memory cell when the masking is released by the data mask signal; and

a control circuit to input data to the first buffer by controlling said data receive gate according to a write enable signal and the data mask signal in a present cycle, and input the data of the first buffer to the second buffer by controlling said data transfer gate and then output the data in the second buffer to said data bus by controlling said data write gate in a subsequent cycle,

wherein, in said cycle of said control circuit, data is not inputted to the first buffer by controlling the data receive gate, and at the same time data is inputted to the second buffer by controlling the data transfer gate, in a certain

cycle depending on a time period from activation of the write enable signal to changing of the data mask signal.

2. The memory device according to claim 1, wherein, in said cycle of said control circuit, data is not inputted to said first buffer by said data receive gate control, while data is inputted to said second buffer by said data transfer gate, and the data in the second buffer is outputted to said data bus by said control of data write gate.

3. The memory device according to claim 1, wherein, in said cycle of said control circuit, data is not inputted to the first buffer by controlling the data receive gate, while data is inputted to the second buffer by controlling the data transfer gate, and the data in the second buffer is not outputted to the data bus by controlling the data write gate.

4. The memory device according to claim 1, wherein, in said cycle of said control circuit, said selector does not connect the data bus to the memory cell in a subsequent cycle, when data is not inputted to the first buffer by controlling the data receive gate, and inputted to the second buffer by controlling the data transfer gate.

5. The memory device according to claim 1, wherein, in said control circuit when the data in the second buffer is outputted to the data bus by controlling the data write gate, data is always

inputted to the second buffer by controlling the data transfer gate within the cycle thereof and before the controlling the data write gate.

6. The memory device according to claim 5, wherein, in said control circuit, depending on a time period from activation of the write enable signal to changing of the data mask signal, in the cycle, data is inputted to the second buffer by controlling the data transfer gate, and data is not outputted to the data bus by controlling data write gate.

7. The memory device according to claim 1, further comprising:

a first delay circuit to generate a first signal according to the write enable signal and the data mask signal, and output, as a first delay signal, a signal which delays, for a first delay time period, a changing point at which the first signal changes from a deactivated state to an activated state;

a second delay circuit to output, as a second delay signal, a signal which delays, for a second delay time period which is longer than said first delay time period, a changing point at which the first signal changes from a deactivated state to an activated state; and

wherein, in said control circuit, the data transfer gate is controlled by pulse at the changing point at which said fist delay signal changes from the deactivated state to the activated state, whereby

data is inputted to the second buffer, and the data receive gate is controlled by pulse at the changing point at which the second delay signal changes from the activated state to the deactivated state, whereby data is inputted to the first buffer.

8. The memory device according to claim 7, wherein:

in said first delay circuit, is generated a first signal to activate a period during which the write enable signal is activated and the data mask signal is in a mask-releasing state, and is outputted, as a fist delay signal, a signal which delays, for a first delay time period, a changing point at which the first signal changes from a deactivated state to an activated state;

in said second delay circuit, is outputted, as a second delay signal, a signal which delays, for a second delay time period which is longer than said first delay time period, a changing point at which said first signal changes from a deactivated state to an activated state; and

in said control circuit, data is inputted to the second buffer by controlling the data transfer gate by pulse at a changing point at which the first delay signal changes from a deactivated state to an activated state, and data is outputted to the first buffer by controlling the data receive gate by pulse at a changing point at which the second delay signal

changes from an activated state to a deactivated state.

9. The memory device according to claim 1, wherein, in a cycle in which the activation period of the write enable signal is short, data is inputted to the second buffer by controlling the data transfer gate, and at the same time not inputted to the first buffer by controlling the data receive gate.

10. The memory device according to claim 1, further comprising:

a mask receive gate to buffer, in a first mask buffer, a data mask signal inputted by gate control;

a mask transfer gate to input a data mask signal of said first mask buffer and buffer the same signal in a second mask buffer; and

a mask write gate to output to said selector the data mask signal in said second mask buffer by gate control.

11. The memory device according to claim 1, wherein said data mask signal comprises an upper byte mask signal and a lower byte mask signal.

12. The memory device according to claim 4, wherein, in said cycle of said control circuit, data is not inputted to said first buffer by controlling the data receive gate, while data is inputted to said second buffer by controlling said data transfer gate, and the data in the second buffer is outputted to the data bus by controlling said data write gate.

13. The memory device according to claim 12, wherein, in said cycle of said control circuit, data is not inputted to the first buffer by controlling the data receive gate, while data is inputted to the second buffer by controlling the data transfer gate, and the data in the second buffer is not outputted to the data bus by controlling the data write gate.

14. The memory device according to claim 13, wherein, in the control circuit, when the data in the second buffer is outputted to the data bus by controlling the data write gate, data is always inputted to the second buffer by controlling the data transfer gate in the cycle thereof and before the controlling the data write gate.

15. The memory device according to claim 14, wherein, in said control circuit, data is inputted to the second buffer by controlling the data transfer gate and at the same time is not inputted to the data bus by controlling the data write gate, depending on the time period from the activation of the write enable signal to the changing of the data mask signal in the cycle thereof.

16. The memory device according to claim 15, further comprising:

a first display circuit to generate a first signal according to the write enable signal and the data mask signal, and output, as a first delay signal, a signal which delays, for a first delay time period,

a changing point at which said first signal changes from a deactivated state to an activated state; and

a second delay circuit to output, as a second delay signal, a signal which delays, for a second time period which is longer than the first time period, a changing point at which said first signal changes from a deactivated state to an activated state,

wherein, in said control circuit, data is inputted to the second buffer by controlling the data transfer gate by pulse at an changing point at which the first delay signal changes from a deactivated state to an activated state, and data is inputted to the first buffer by controlling the data receive gate by pulse at an changing point at which the second delay signal changes from an activated state to a deactivated state.

17. The memory device according to claim 16, wherein:

in said first delay circuit, is generated a first signal which activates a period during which the write enable signal is activated and the data mask signal is in mask-releasing state, and is outputted, as a first delay signal, a signal which delays, for a first delay time period, an changing point at which the first signal changes from a deactivated state to an activated state;

in said second delay circuit, is outputted, as a second delay signal, a signal which delays, for a second delay time period which is longer than said first delay time period, a changing point at which said first signal changes from a deactivated state to an activated state; and

in said control circuit, data is inputted to the second buffer by controlling the data transfer gate by pulse at a changing point at which the first delay signal changes from a deactivated state to an activated state, and data is inputted to the first buffer by controlling the data receive gate by pulse at a changing point at which the second delay signal changes from an activated state to a deactivated state.

18. The memory device according to claim 17, wherein, in said control circuit, data is inputted to the second buffer by controlling the data transfer gate and is not inputted to the second buffer by controlling the data receive gate, in a cycle where the activation period of the write enable signal is short.

19. The memory device according to claim 18, further comprising:

a mask receive gate to buffer, in a first mask buffer, a data mask signal inputted by gate control;

a mask transfer gate to input the data mask signal of said first mask buffer and buffer the same signal in a second mask buffer, by gate control; and

a mask write gate to output the data mask signal in said second mask buffer to said selector by gate control.

20. The memory device according to claim 19, wherein said data mask signal comprises an upper byte mask signal and a lower byte mask signal.